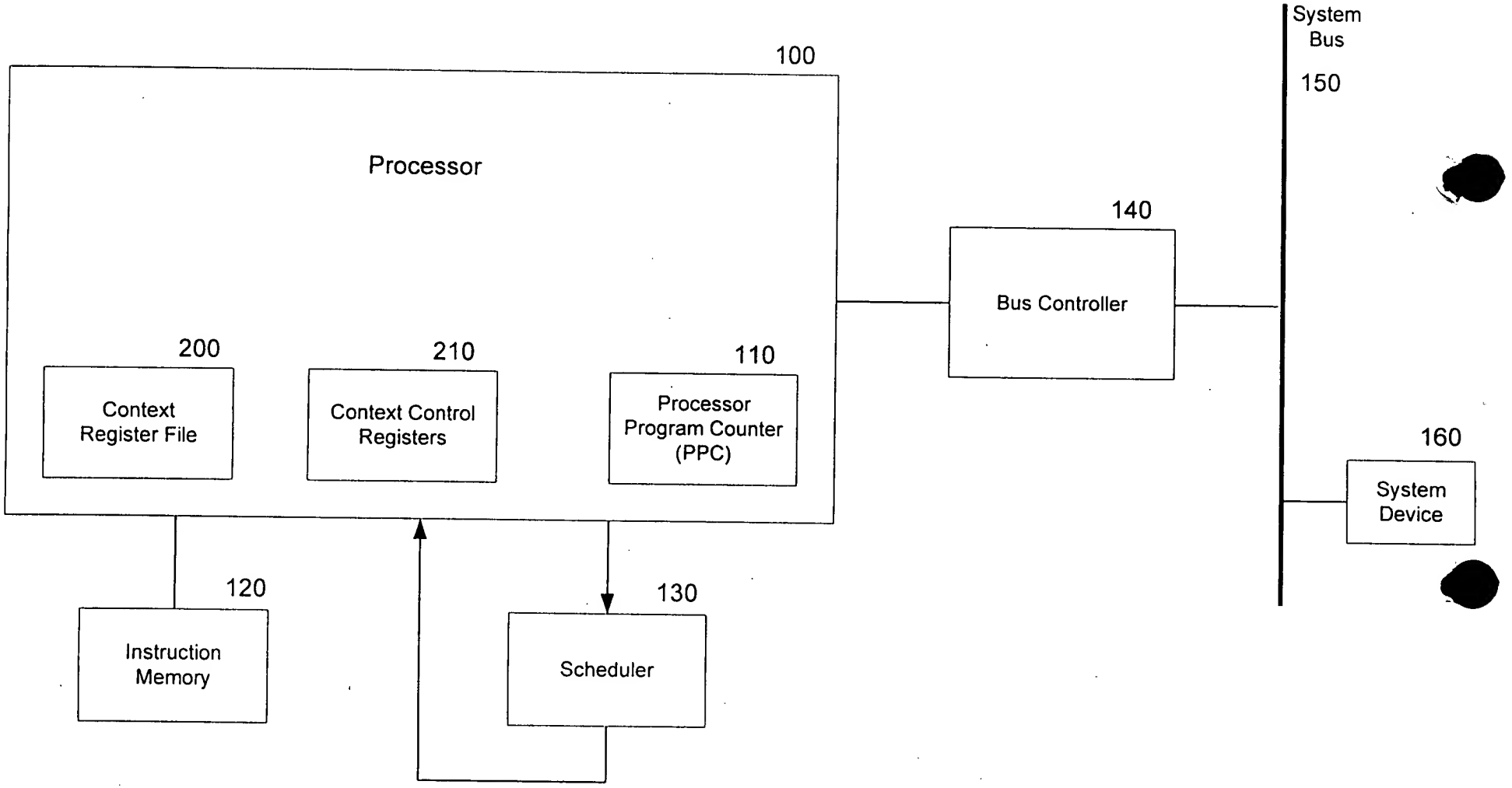


Fig. 1

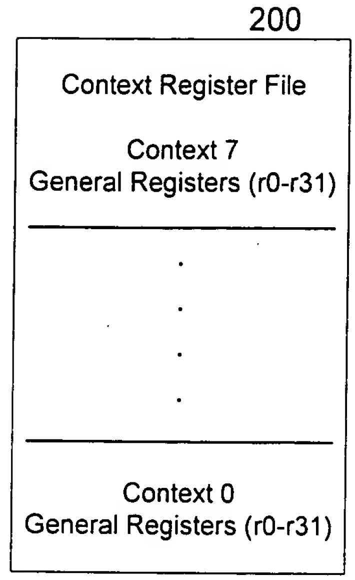


Fig. 2a

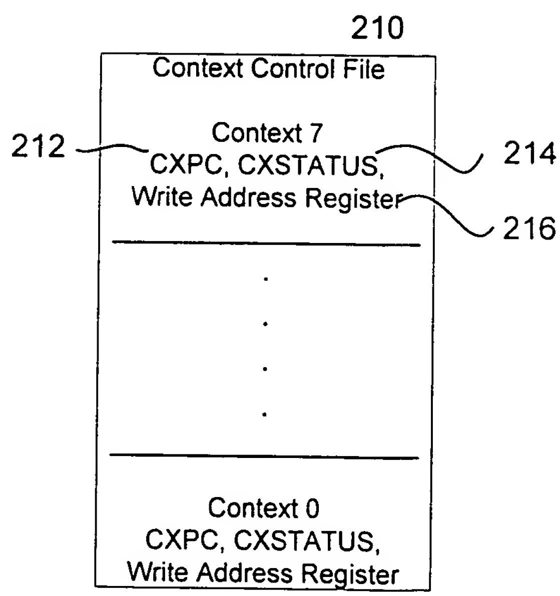


Fig. 2b

300

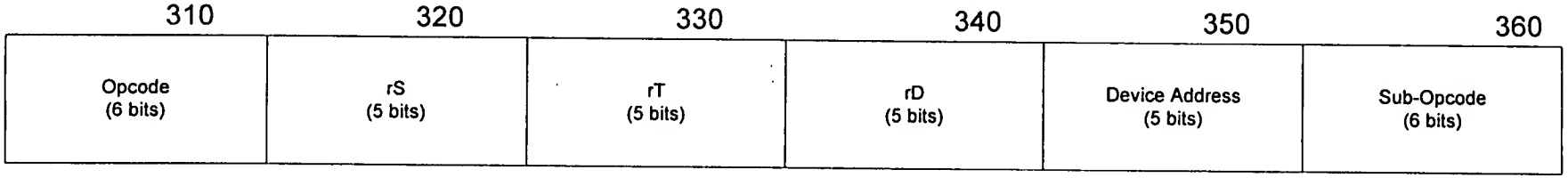


Fig. 3

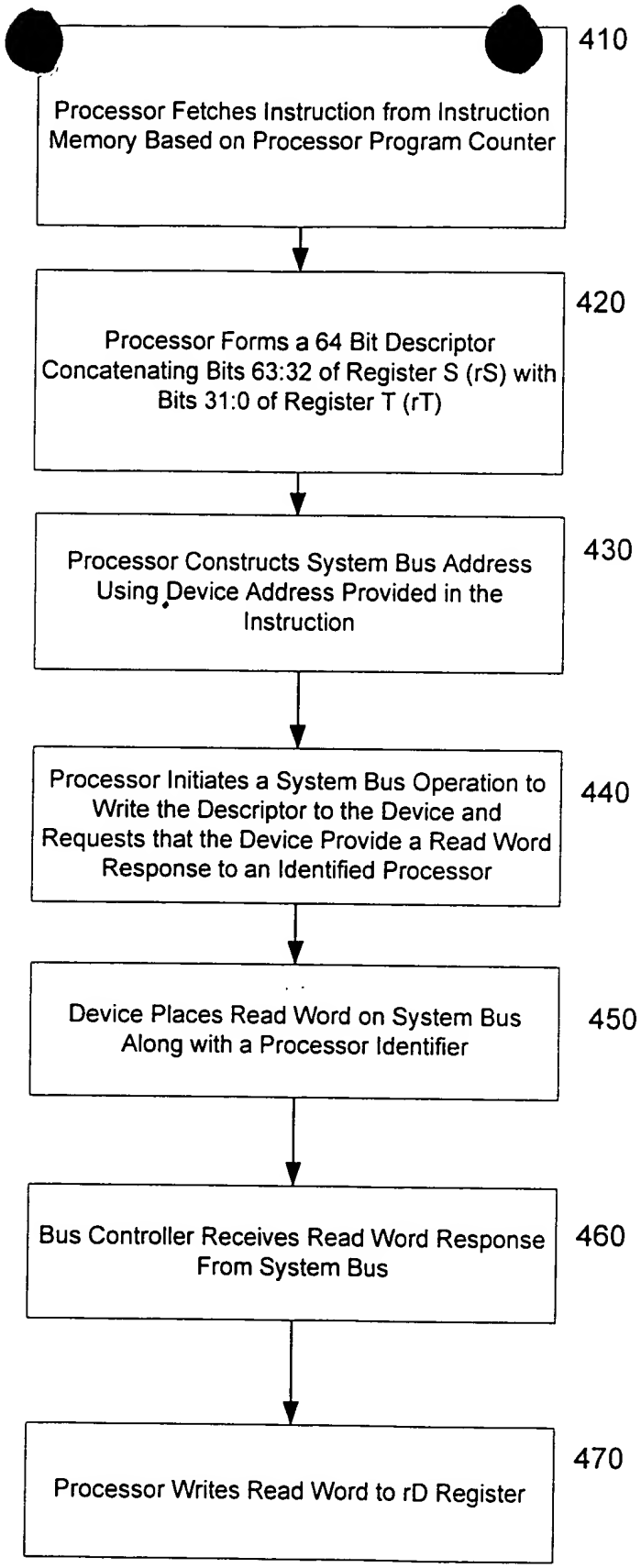
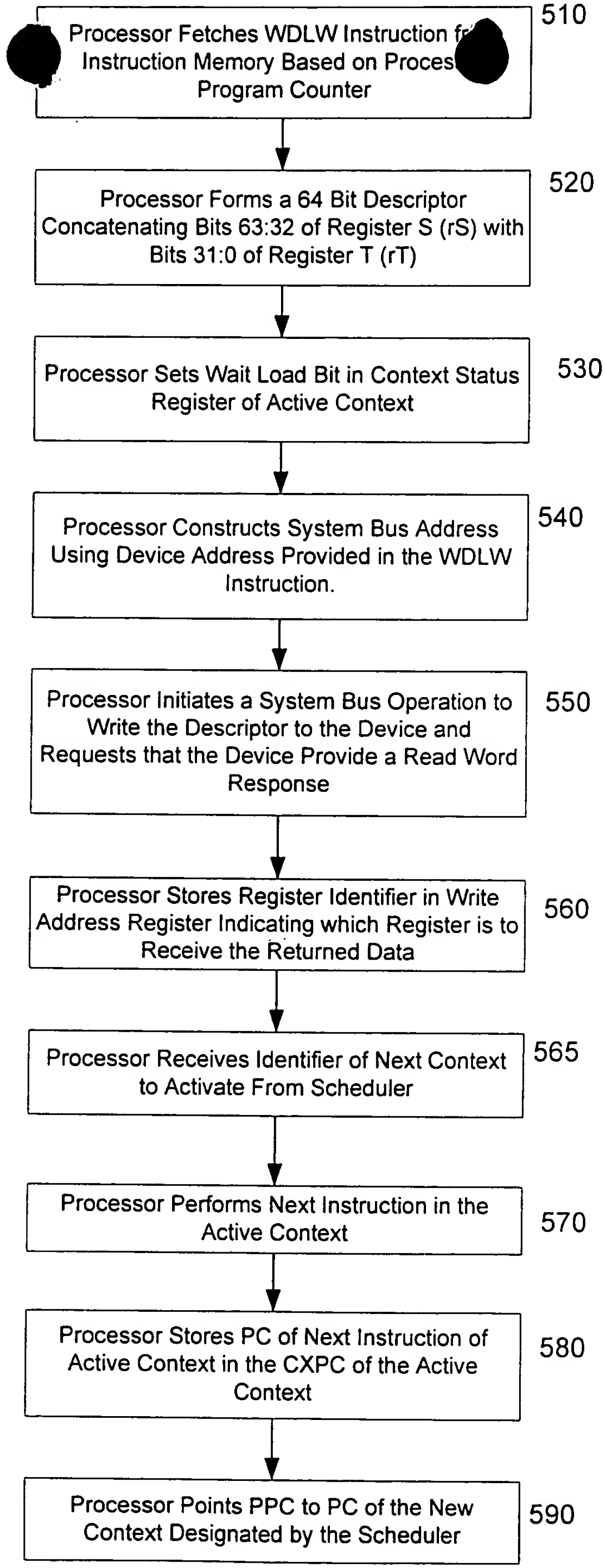

400
410
Processor Fetches Instruction from Instruction Memory Based on Processor Program Counter
420
Processor Forms a 64 Bit Descriptor Concatenating Bits 63:32 of Register S (rS) with Bits 31:0 of Register T (rT)
430
Processor Constructs System Bus Address Using Device Address Provided in the Instruction
440
Processor Initiates a System Bus Operation to Write the Descriptor to the Device and Requests that the Device Provide a Read Word Response to an Identified Processor
450
Device Places Read Word on System Bus Along with a Processor Identifier
460
Bus Controller Receives Read Word Response From System Bus
470
Processor Writes Read Word to rD Register

Fig. 4

500



Processor Fetches WDLW Instruction fr
Instruction Memory Based on Proces
Program Counter
510
Processor Forms a 64 Bit Descriptor Concatenating Bits 63:32 of Register S (rS) with Bits 31:0 of Register T (rT)
520
Processor Sets Wait Load Bit in Context Status Register of Active Context
530
Processor Constructs System Bus Address Using Device Address Provided in the WDLW Instruction.
540
Processor Initiates a System Bus Operation to Write the Descriptor to the Device and Requests that the Device Provide a Read Word Response
550
Processor Stores Register Identifier in Write Address Register Indicating which Register is to Receive the Returned Data
560
Processor Receives Identifier of Next Context to Activate From Scheduler
565
Processor Performs Next Instruction in the Active Context
570
Processor Stores PC of Next Instruction of Active Context in the CXPC of the Active Context
580
Processor Points PPC to PC of the New Context Designated by the Scheduler
590

Fig. 5

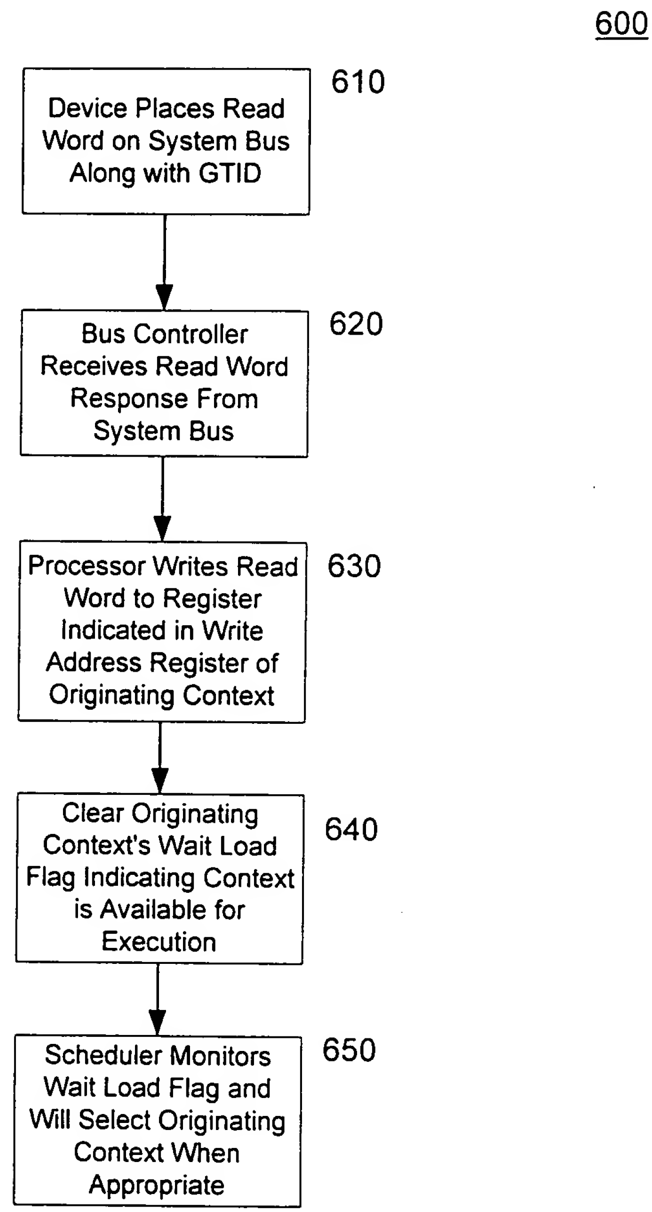


Fig. 6